SOI CMOS DEVICE WITH REDUCED DIBL

Abstract of the Disclosure

CMOS devices formed with a Silicon On Insulator (SOI) technology with reduced Drain Induced Barrier Lowering (DIBL) characteristics and a method for producing the same. The method involves a high energy, high dose implant through openings in a masking layer and through channel regions of the p- and n-wells, into the insulator layer, thereby creating a borophosphosilicate glass (BPSG) diffusion source within the insulation layer underlying the gate regions of the SOI wafer substantially between the source and drain. Backend high temperature processing steps induce diffusion of the dopants contained in the diffusion source into the p- and n-wells, thereby forming asymmetric retrograde dopant profiles in the channel under the gate. The method can be selectively applied to selected portions of a wafer to tailor device characteristics, such as for memory cells.

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